STATUS of DSP FIRMWAREs for EXOGAM2

16 CHANNELS ADCs
RAW DATA
= 44.8Gb/s

DIGITAL SIGNAL PROCESSING

EMBEDDED SOFTWARE
SETUP + READOUT + GTS LEAF

VIRTEX 6 → VIRTEX 5 → EXOGAM2 DATA FLOW < 100Mb/s → ETHERNET

DIGITAL SIGNAL PROCESSING (number)

- ✓ DIGITAL CONSTANT FRACTION DISCRIMINATOR (4)
- ✓ ENERGY (16)
- ✓ TIMING (2)
- ✓ RISE TIME (2)
- ✓ MIRROR CHARGE (8)

STATUS of VIRTEX6 FIRMWARE

- ✓ DEVELOPMENT & EXTENSIVE TESTS => COMPLETED
- ✓ last version : EXPLOITATION 6.46 (28th june 2016)

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SPECIFIC FIRMWARE of VIRTEX6 FPGA DSP for GANIL USE -> UNIFIED FIRMWARE

TYPE of DETECTOR	EXPERIMENT	DSP	NUMBER of CHANNELS Per NUMEXO2	FRAME SIZE (BYTE)	COUNTING RATE Per NUMEXO2	NUMBER of TRs
POSITION DETECTORs	VAMOS	✓ ENERGY (average filter)	2048 (max) multiplexed	280	< 10kHz	1
IONIZATION CHAMBERs	VAMOS	✓ ENERGY (trapezoidal filter) ✓ TRIGGER (dCFD)	16	32	< 10kHz	16
	LISE				1MHz (with inhibit window)	

UNIFIED FIRMWARE of FPGA DSP

- ✓ DEVELOPMENT -> COMPLETED
- ✓ EXTENSIVE TESTS -> IN PROGRESS
- ✓ READY for EXPERIMENT -> 1T 2017

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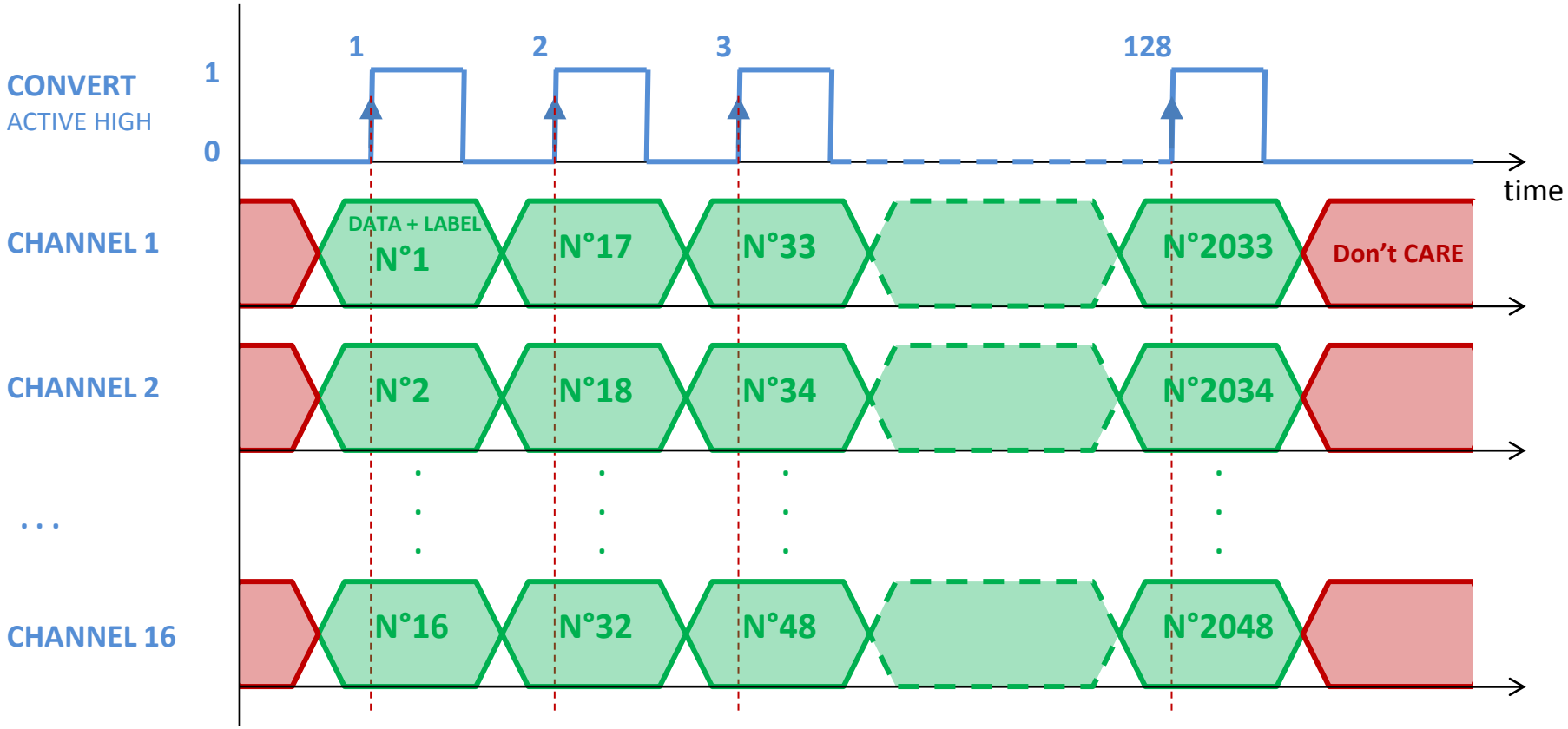
POSITION DETECTOR -> MULTIPLEXED ENERGYs

ONE ENERGY DATA ON EACH EDGE of CONVERT SIGNAL

- ✓ NUMBER OF EDGE => 64, 96 or 128 multiplexed data stream on each NUMEXO2 channel
- ✓ 16 channels => 16 x 128 = 2048 data MAX
- ✓ THRESHOLD and OFFSET for each data



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280B FRAME SPECIFICATION'S for POSITION DETECTORS

	bit [15]	bit [8]	bit [7]	bit [0]	
FRAME TYPE & SIZE	METATYPE = 0x42		FRAMESIZE [23..16] = 0x00		N°1
	FRAMESIZE [15..0] = 0x0046 => 70 word de 32 bits				
	SUBSYSTEM => register IDENTIFICATION*		FRAMETYPE [15..8] = 0x00		
	FRAMETYPE [7..0] = 0x15		REVISION = 0x00		
EVENT NUMBER TIMESTAMP (ADDED to GTS LEAF on V5 FPGA)	EVENTNUMBER [31..16] = 0x0000				
	EVENTNUMBER [15..0] = 0x0000				
	TIMESTAMP [47..32] = 0x0000				
	TIMESTAMP [31..16] = 0x0000				
	TIMESTAMP [15..0] = 0x0000				
IDENTIFICATION	CRISTAL ID	CRISTAL ID[15..5] => board index => register IDENTIFICATION* CRISTAL ID[4..0] = 0x0			
64 DATA of ENERGY LABEL + DATA	HIT CHANNEL LABEL N°1 or 0xFFFF without hit channel				
	ENERGY DATA for HIT CHANNEL LABEL N°1 or 0x0000 without hit channel				
	HIT CHANNEL LABEL N°2 or 0xFFFF without hit channel				
	ENERGY DATA for HIT CHANNEL LABEL N°2 or 0x0000 without hit channel				
	...				
	HIT CHANNEL LABEL N°64 or 0xFFFF without hit channel				
	ENERGY DATA for HIT CHANNEL LABEL N°64 or 0x0000 without hit channel				
	LOCAL COUNTER (16 bits) INSIDE V6 => same value for MULTIPLE FRAMEs				
CHEKSUM	CHECKSUM				N°140

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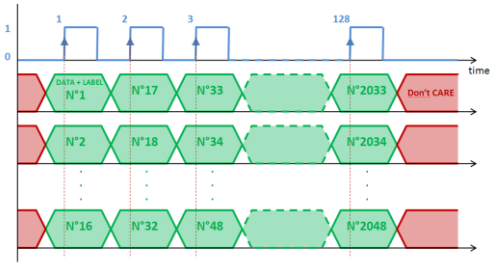
POSITION DETECTOR -> ADAPTATIVE DATA FLOW with FIXED LENGTH FRAME of 280 BYTEs

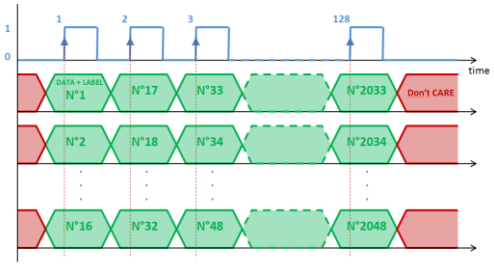
✓ **Standard CASE** -> EACH multiplexed data stream (2048 channels MAX) produces ONE DATA FRAME



0 to 64 DATAs

1 FRAME of 0 to 64 DATA
but FIXED FRAME SIZE of 280B

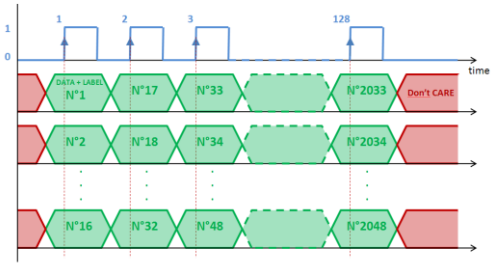
✓ **Specific CASE** -> EACH multiplexed data stream can produce MORE THAN ONE DATA FRAME



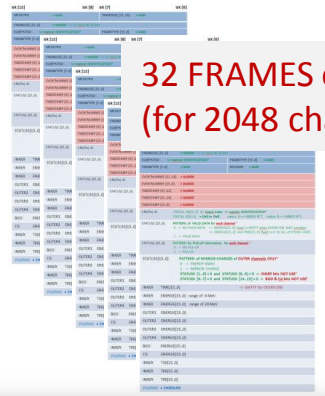
> 64 DATA

2 to 32 FRAMES of 64 DATA
with SAME EVENT NUMBER

✓ **Specific CASE** -> CALIBRATION



ALL DATA



32 FRAMES of 64 DATA
(for 2048 channels)

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32B FRAME SPECIFICATION for IONIZATION CHAMBERS

	bit [15]	bit [8]	bit [7]	bit [0]	
FRAME TYPE & SIZE	METATYPE = 0x42		FRAMESIZE [23..16] = 0x00		N°1
	FRAMESIZE [15..0] = 0x0008 => 8 word de 32 bits				
	SUBSYSTEM => register IDENTIFICATION*		FRAMETYPE [15..8] = 0x00		
	FRAMETYPE [7..0] = 0x14		REVISION = 0x00		
EVENT NUMBER TIMESTAMP (ADDED to GTS LEAF on V5 FPGA)	EVENTNUMBER [31..16] = 0x0000				
	EVENTNUMBER [15..0] = 0x0000				
	TIMESTAMP [47..32] = 0x0000				
	TIMESTAMP [31..16] = 0x0000				
	TIMESTAMP [15..0] = 0x0000				
IDENTIFICATION	CRISTAL ID	CRISTAL ID[15..5] => register IDENTIFICATION* => BOARD INDEX CRISTAL ID[4..0] = 0x0 to 0xF valeur 0 => VOIE N°1 ... valeur 15 => VOIE N°16			
STATUS for 1 CHANNEL ✓ VALID DATA ✓ PILE-UP	STATUS1 [0]	PATTERN of VALID DATA 0 -> NO VALID DATA => ENERGIE[15..0] fixed to 0 1 -> VALID DATA			
	STATUS2 [0]	PATTERN for PILE-UP information 0 -> NO PILE-UP 1 -> PILE-UP			
1 DATA of ENERGY	= 0x0000				
	ENERGIE sur 16 bits				
	= 0x0000				
CHEKSUM	CHECKSUM				N°16

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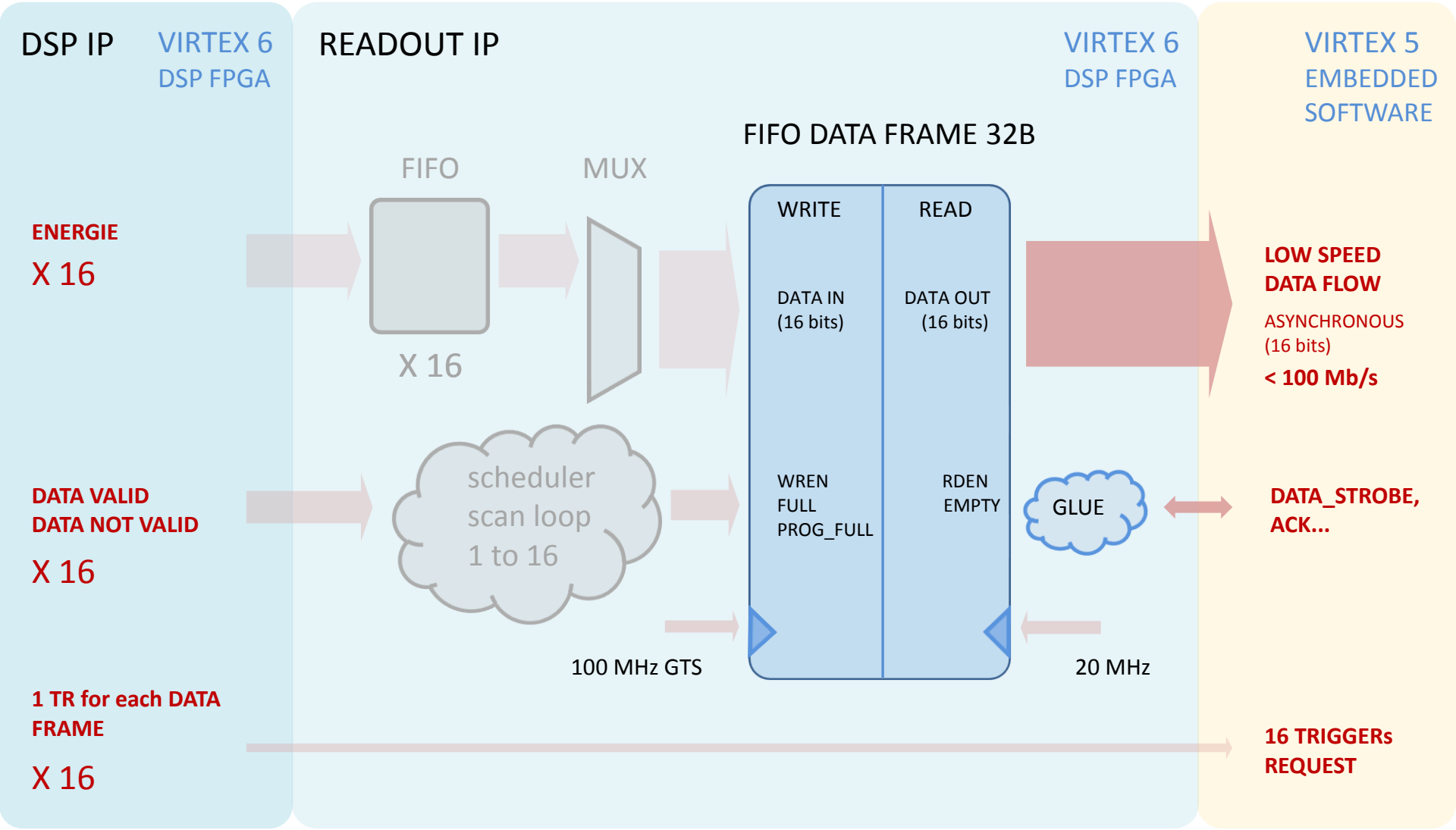
READOUT IP for IONIZATION CHAMBERS -> 16 DATA producers



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DIAGNOSTICS & INSPECTIONS -> highly recommended IPs to be added to your FIRMWAREs

TESTs all DATA TRANSMISSION from FADCs -> VIRTEX6

112 links@400Mb/s

FADCs pattern injected

GUI GECO

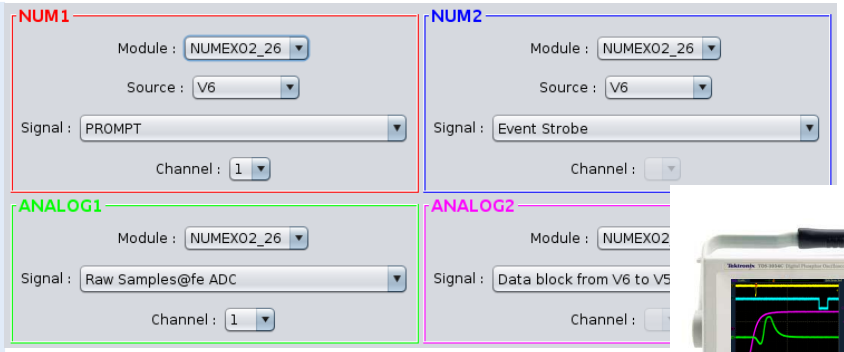
IP_ISERDES/IP_TEST_LIENS_FADC

VIRTEX6 resources (SLICES) **< 1%**

INSPECTIONS lines

LOGICALs (2X)

ANALOGs@200Msps (2X)



IPs_INSPECTIONS/INSPECTIONS_LOGIQUES

IPs_INSPECTIONS/DAC_INSPECTIONS

VIRTEX6 resources (SLICES) **≈ 4%**

FRONT PANEL NUMEXO2
lines can be chained
(test by chaining 16 NUMEXO2)

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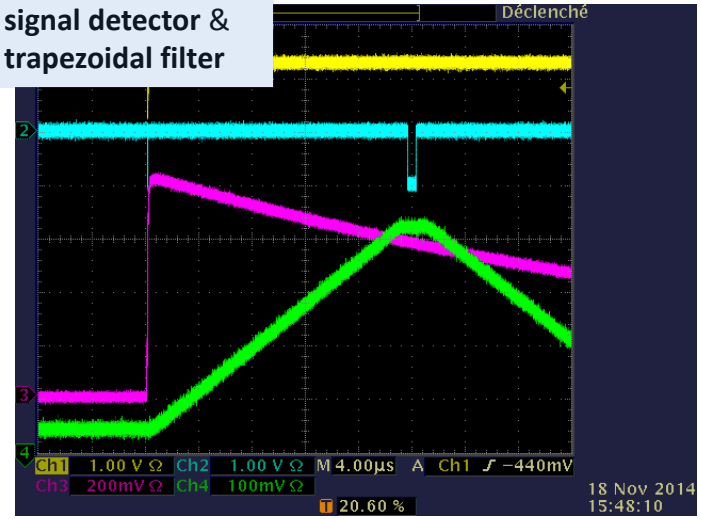
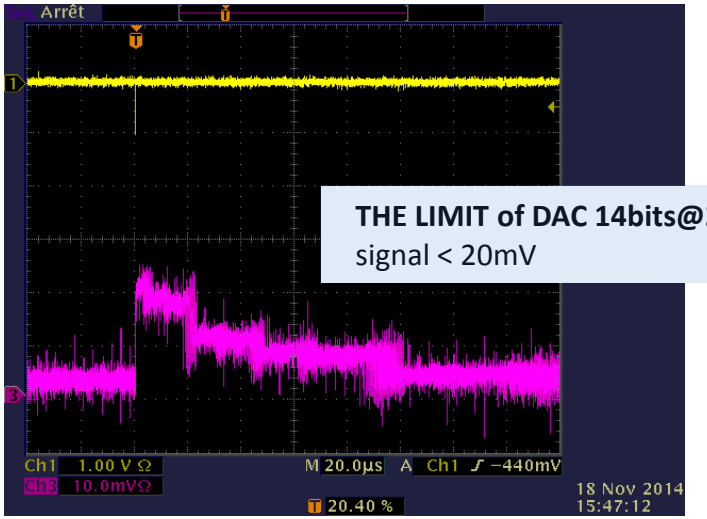
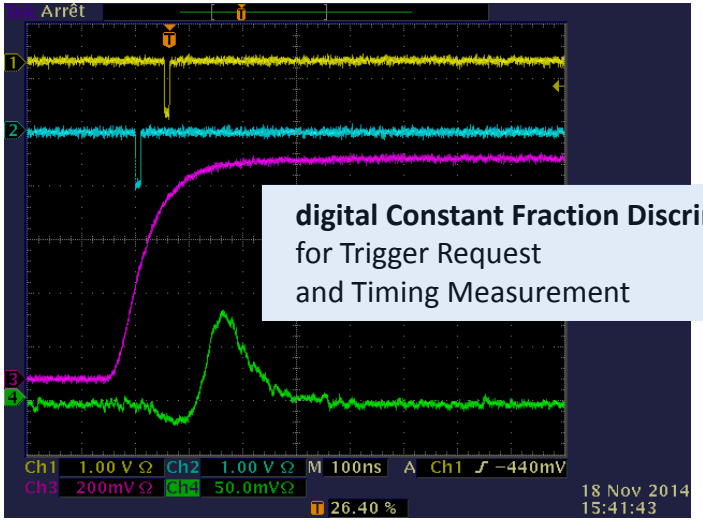
INSPECTIONS examples with EXOGAM2 FIRMWARE (ALL version)

signal detector &
trapezoidal filter

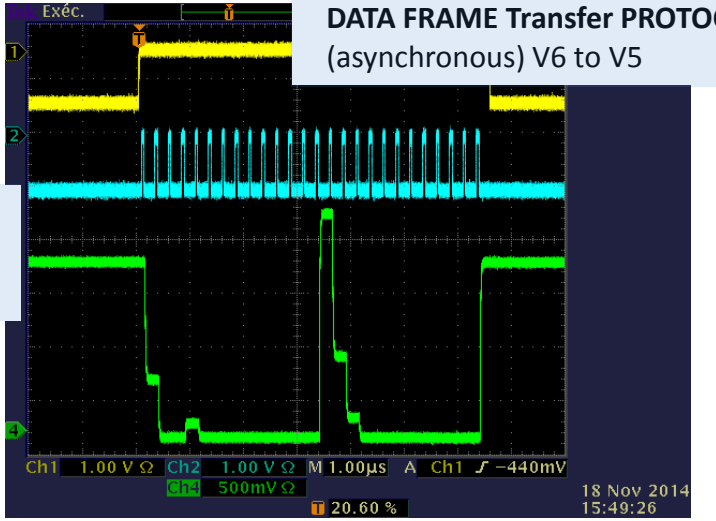




THE LIMIT of DAC 14bits@200Msps
signal < 20mV



digital Constant Fraction Discriminator
for Trigger Request
and Timing Measurement



DATA FRAME Transfer PROTOCOL
(asynchronous) V6 to V5

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DIAGNOSTICS & INSPECTIONS -> highly recommended IPs to be added to your FIRMWAREs

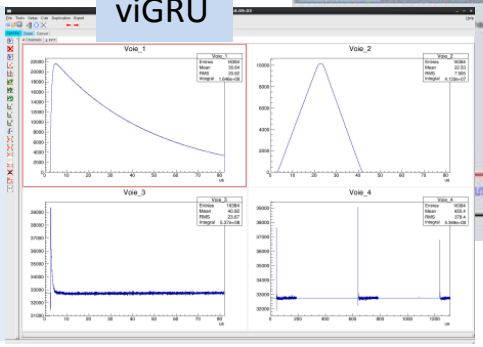
MODE SCOPE @retinian persistence

4 circulars buffers @200Msps

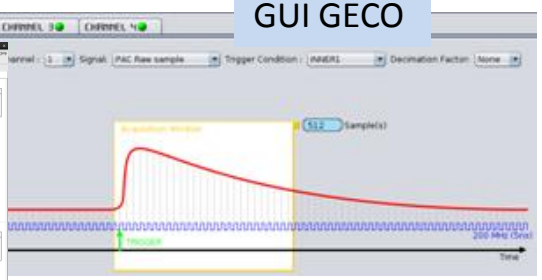
IP_OSCILLOSCOPE

VIRTEX6 resources (SLICES) ≈ **4%**

viGRU



GUI GECO

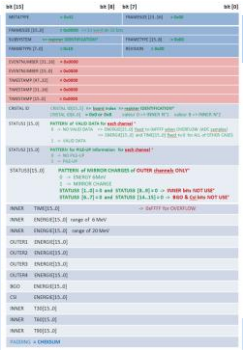


double CHECK INTEGRITY of all HEADER FRAMEs for producer & consumer

+ CHECKSUM

IP_BLOC_DONNEES_EVT (dedicated FSM)

VIRTEX6 resources (SLICES) **< 1%**



HEADER

CHECKSUM

SCALERs (number of PROMPTs, TRs, ERROR FRAMEs...)

thru SPI SETUP link (READ each second)

IP_SETUP_SPI

VIRTEX6 resources (SLICES) ≈ 2%

GUI GECO

NUMEXO2_38

Name	Counting frequency
INNER_1 TRIG	3578408144
INNER_1 TRIG_REQ	2592252903
INNER_1 TRIG_REQ Valid Data	2464788647
INNER_1 TRIG_REQ No Valid Data	127464256
INNER_2 TRIG	3578408376
INNER_2 TRIG_REQ	2592255307
INNER_2 TRIG_REQ Valid Data	2464793457
INNER_2 TRIG_REQ No Valid Data	127461850
OUTER_1	0
OUTER_2	0
OUTER_3	0
OUTER_4	0
OUTER_5	0
OUTER_6	0
OUTER_7	0
OUTER_8	0
BLOC_DONNEES	889540914
NONE	0
NONE	0
NONE	0

NUMEXO2_37

Name	Counting frequency
INNER_1 TRIG	3578409711
INNER_1 TRIG_REQ	2587720067
INNER_1 TRIG_REQ Valid Data	2037384817
INNER_1 TRIG_REQ No Valid Data	550335250
INNER_2 TRIG	3578410248
INNER_2 TRIG_REQ	2587720610
INNER_2 TRIG_REQ Valid Data	2037385903
INNER_2 TRIG_REQ No Valid Data	550334707
OUTER_1	0
OUTER_2	0
OUTER_3	0
OUTER_4	0
OUTER_5	0
OUTER_6	0
OUTER_7	0
OUTER_8	0
BLOC_DONNEES	880473381
NONE	0
NONE	0
NONE	0

NUMEXO2_

Name	Counting frequency
INNER_1 TRIG	3578484468
INNER_1 TRIG_REQ	2619568244
INNER_1 TRIG_REQ Valid Data	2481330453
INNER_1 TRIG_REQ No Valid Data	138237791
INNER_2 TRIG	3578484992
INNER_2 TRIG_REQ	2619586444
INNER_2 TRIG_REQ Valid Data	2481366852
INNER_2 TRIG_REQ No Valid Data	138219592
OUTER_1	0
OUTER_2	0
OUTER_3	0
OUTER_4	0
OUTER_5	0
OUTER_6	0
OUTER_7	0
OUTER_8	0
BLOC_DONNEES	944187392
NONE	0
NONE	0
NONE	0

_O2_35

Name	Counting frequency
INNER_1 TRIG	3578511756
INNER_1 TRIG_REQ	2490409015
INNER_1 TRIG_REQ Valid Data	1681298060
INNER_1 TRIG_REQ No Valid Data	809110955
INNER_2 TRIG	3578512282
INNER_2 TRIG_REQ	2721052342
INNER_2 TRIG_REQ Valid Data	2142584715
INNER_2 TRIG_REQ No Valid Data	578467627
OUTER_1	0
OUTER_2	0
OUTER_3	0
OUTER_4	0
OUTER_5	0
OUTER_6	0
OUTER_7	0
OUTER_8	0
BLOC_DONNEES	916494061
NONE	0
NONE	0
NONE	0

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SHARED FIRMWARE of VIRTEX6 => WHEN & WHO

https://u.ganil-spiral2.eu/cloud

https://www.dropbox.com/home

FIRMWARE or specific IP	DIAMANT	NEDA	PARIS	SIRIUS (CSNSM)	SIRIUS (IRFU)
FULL EXOGAM2 FIRMWARE	EXP 5.72 EXP 6.21 ?	BETA 2.71	BETA 2.71	EXP 5.72	EXP 5.72
IP of TIMING (improved version)	-	EXP 6.21 (part of)	-	-	-
16 independent channels (E + dCFD) 32B FRAME	BASE 1.00	-	-	-	-
FULL UNIFIED FIRMWARE 32B et 280B FRAMES	not available to SHARE				

BETA 2.71	deprecated version -> NUMEXO2 one week training @GANIL 3rd -7th February 2014
EXP 5.72	**REFERENCE version (extensive tests)**
EXP 6.21	improved version for TIMING measurement and TR modulation
EXP 6.46 (last)	improved version to manage BGO/CSI triggers
BASE 1.00	first step towards FULL UNIFIED FIRMWARE for new generic usage (VAMOS, LISE...)

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