NEDA TDC

Status/progress Nov 2016

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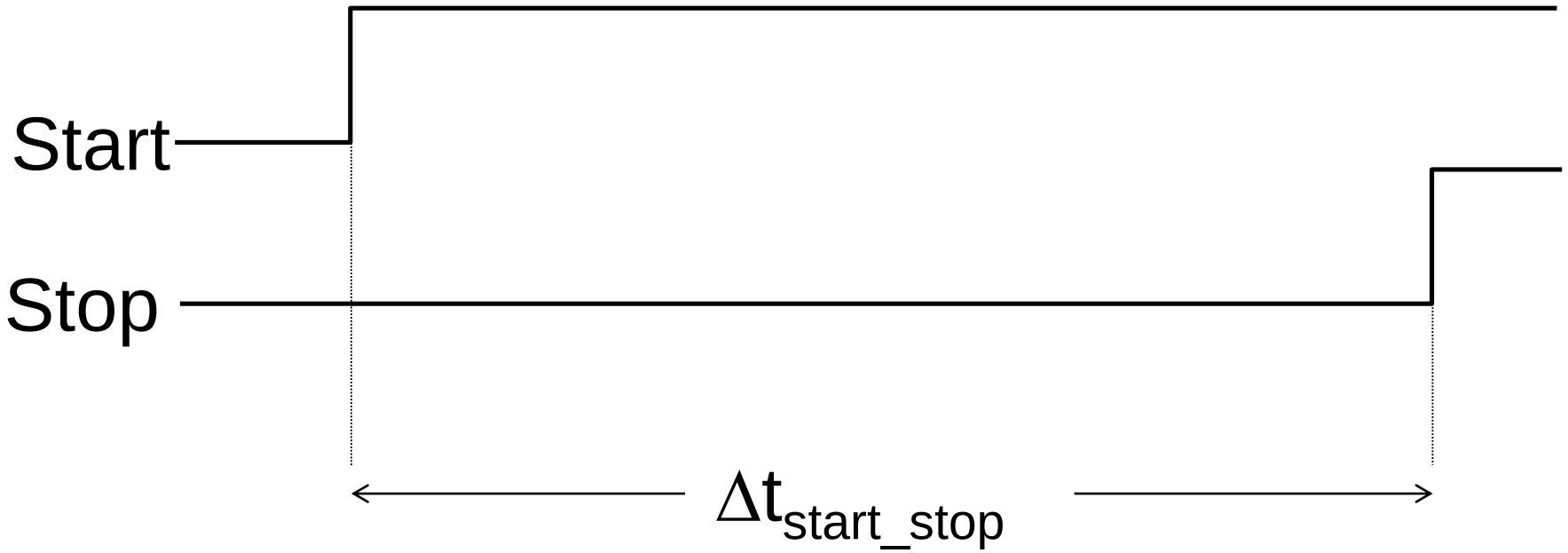
Nuclear Physics Group

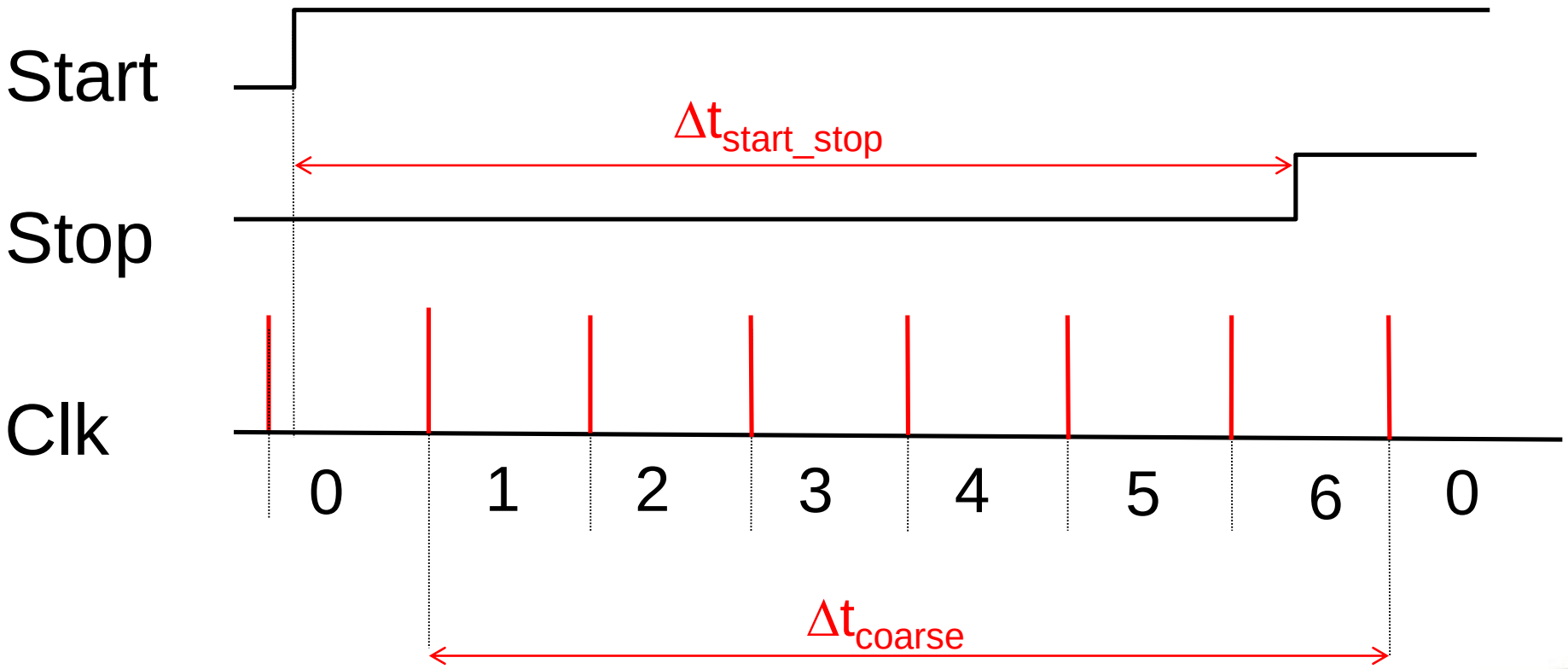
Requirements

- Sub-ns resolution.
- Range 200ns.
- Pile-up is ignored.
- Simple architecture.
- 5ns correction for odd samples.

Neda TDC



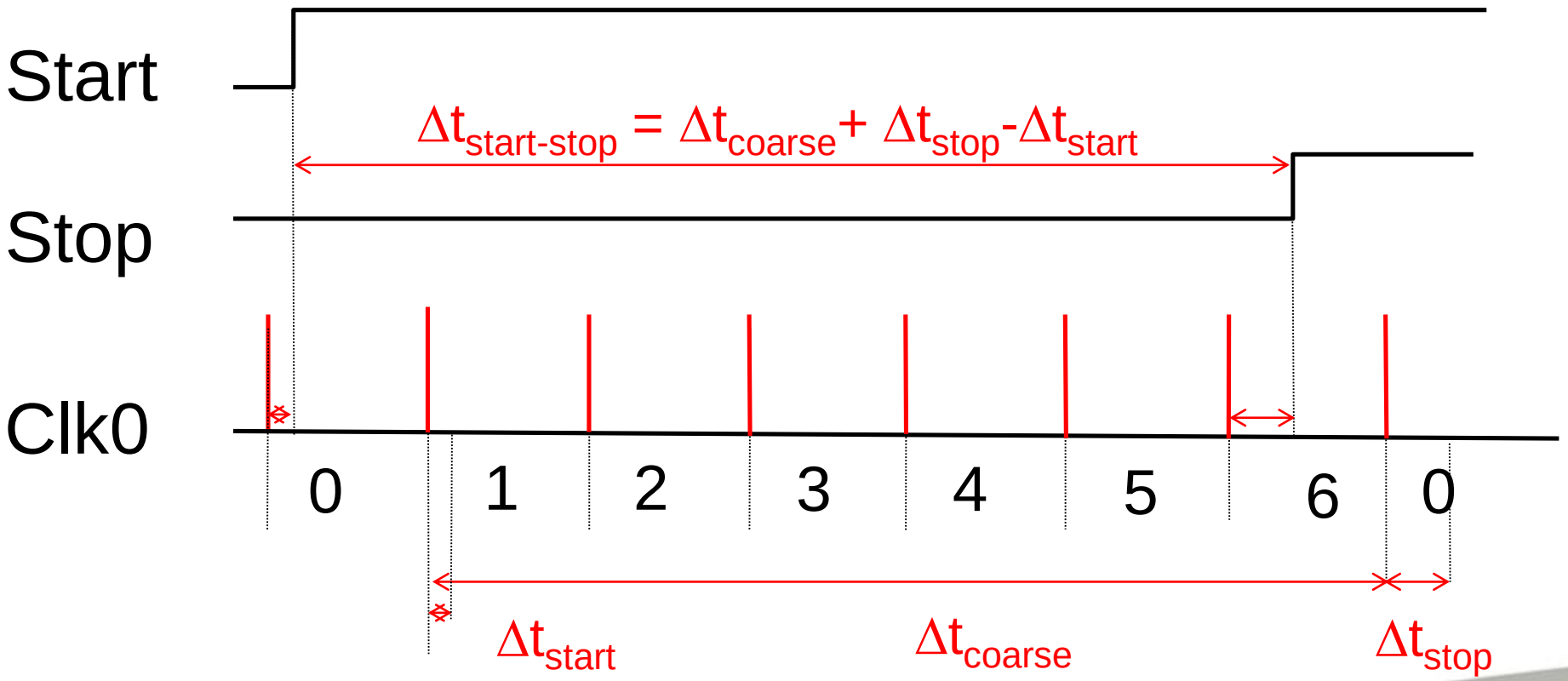
TDC Single Counter



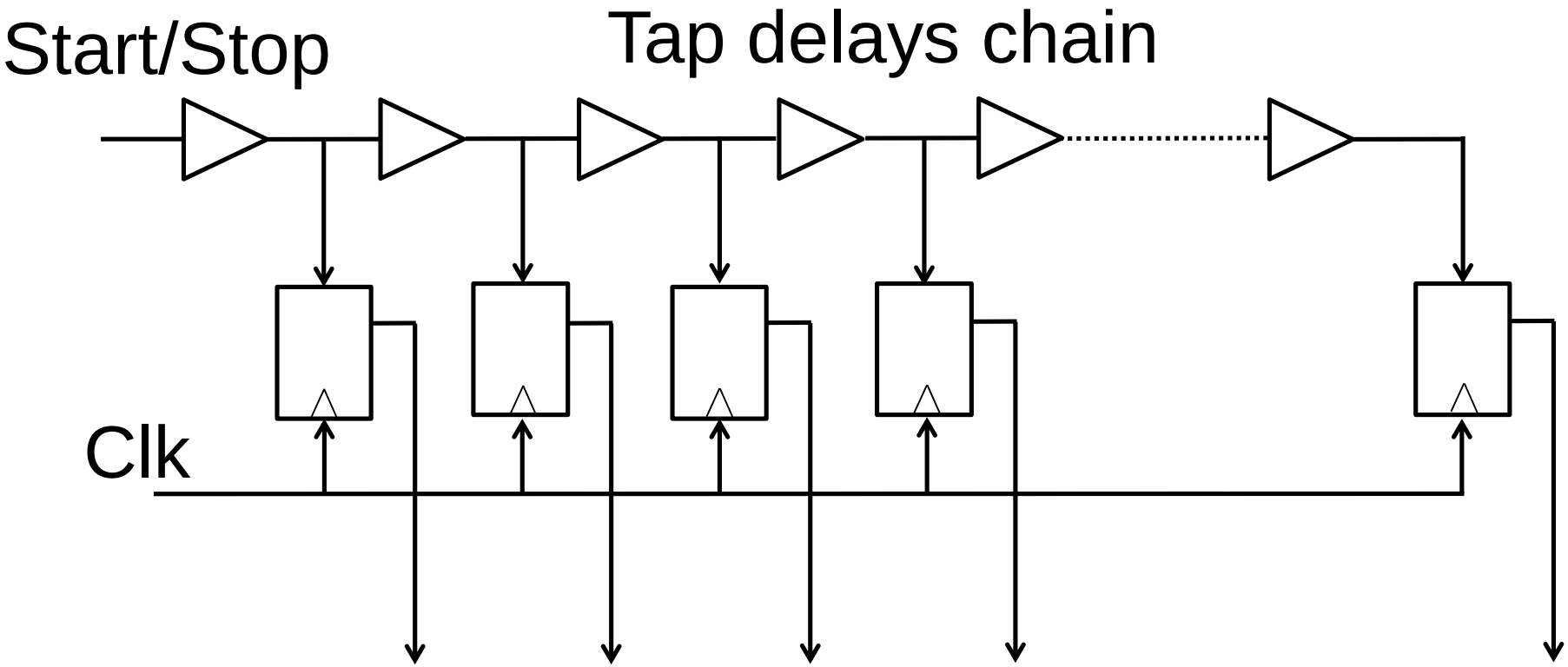
TDC Single Counter

- >1GHz clock required.
- Virtex 6 clk Freq. max = 700MHz.
- Even so, meeting timing closure becomes difficult.

TDC Coarse and Fine Cnt



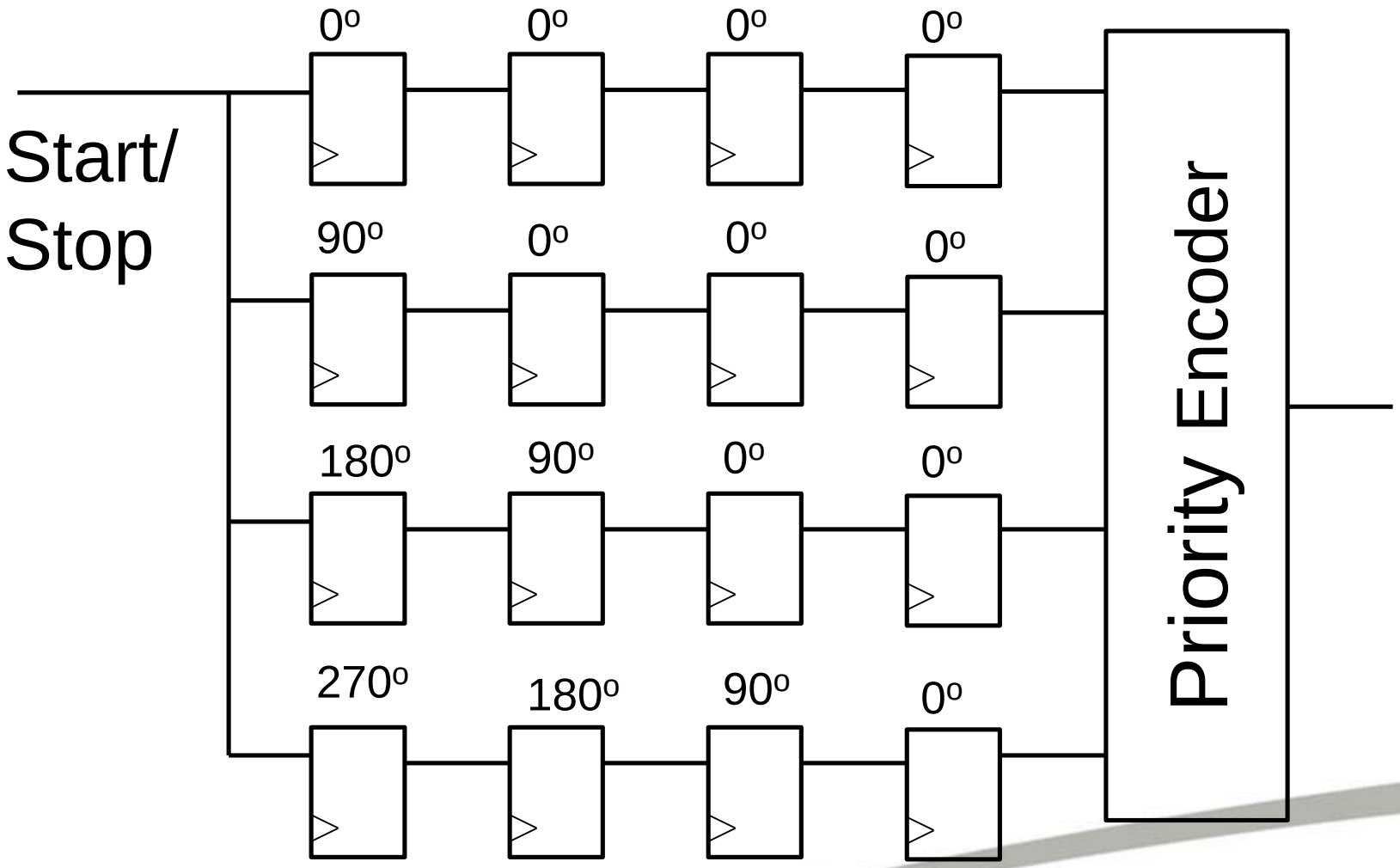
MultiTap Delay



MultiTap Delay Fine Cnt

- Calibration block required for tap delays
- Extra fpga fabric/resources.
- Can achieve very fine resolution (10s of ps).

Multi-Phase Fine Cnt



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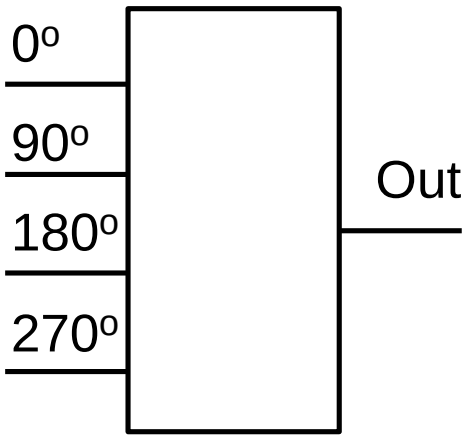
Encoder



0°	90°	180°	270°	Out
1	X	X	X	0
0	1	X	X	1
0	0	1	X	2
0	0	0	1	3

Multi-Phase Fine Cnt

- Clk0 = 300MHz, Clk0/4 prd = 833ps.
- Start/stop is sampled by 4-phases of the same clk (clk0, clk90, clk180, clk270).
- Start/stop async to any of the above clocks.

Multi-Phase Fine Cnt

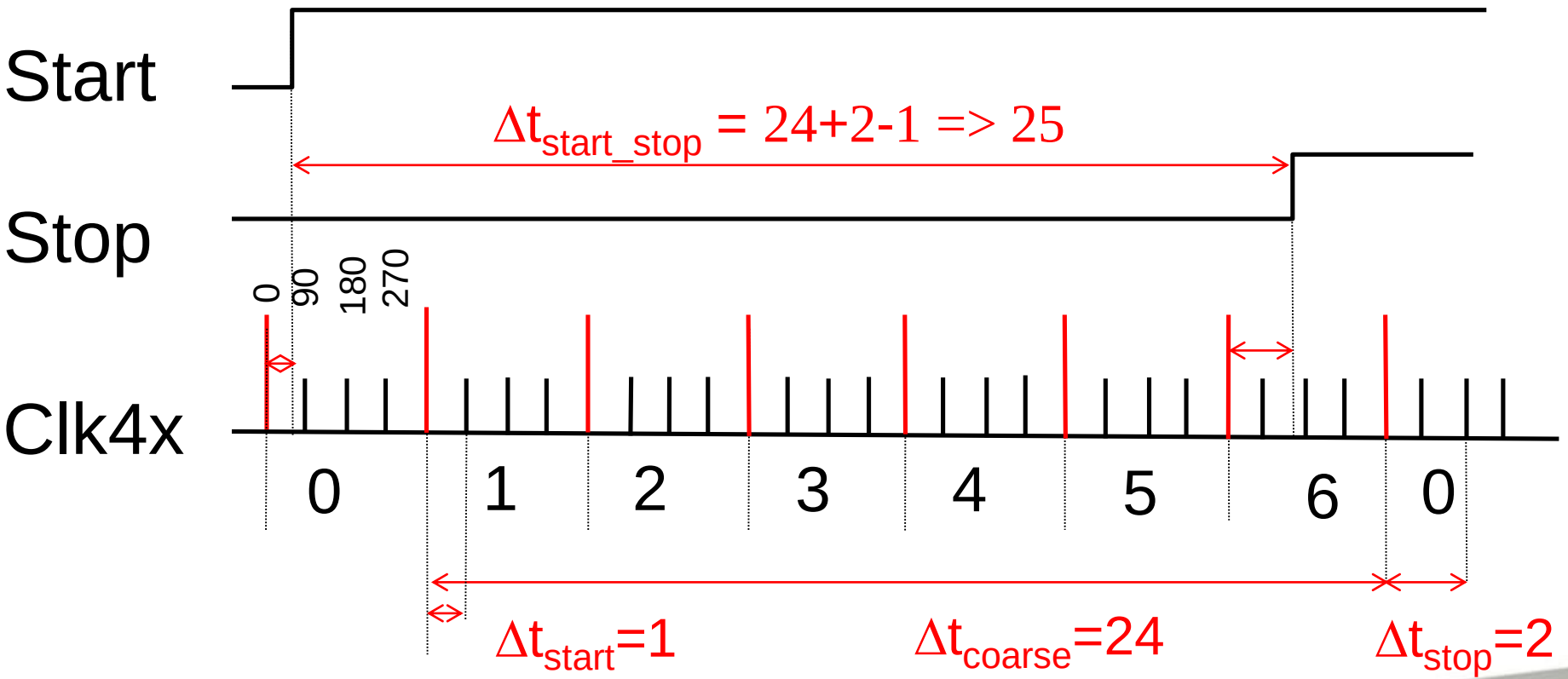
- Require 2 clock domains, for clk0 and clk90. FFs that use the clk180 and clk270 are clked by the falling edge of the clk0 and clk90.

- “Counts” how many clk0/4 periods are from the rising edge of clk0 to the rising edge of start/stop (range 0-3).

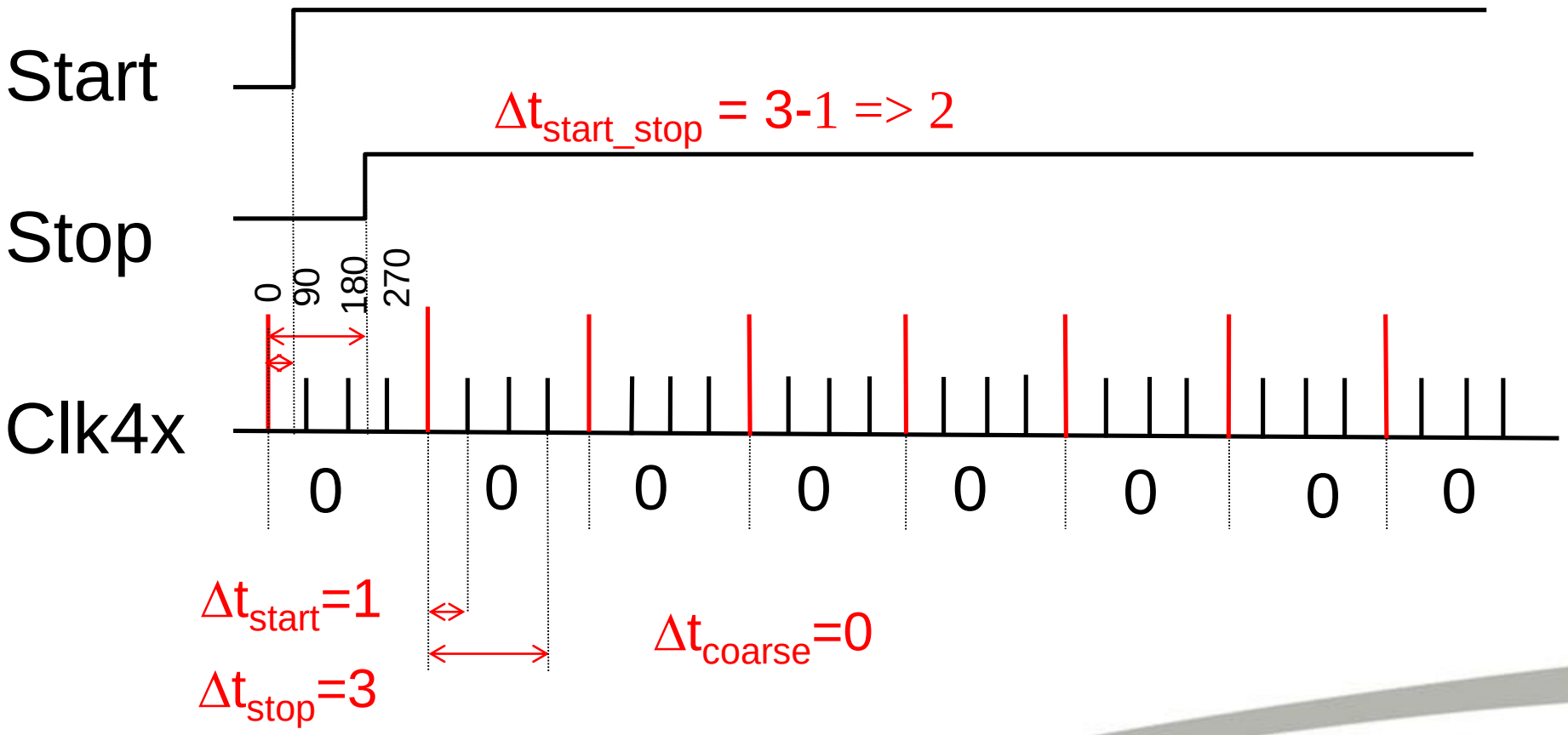
Encoder

- Priority Encoder will work ok, if start (or stop) min. repetition time is 2 clk0 cycles.
- Start is generated by 100MHz and is 1 clk cycle wide => min. rep. = 20ns.
- Stop min. repetition time?

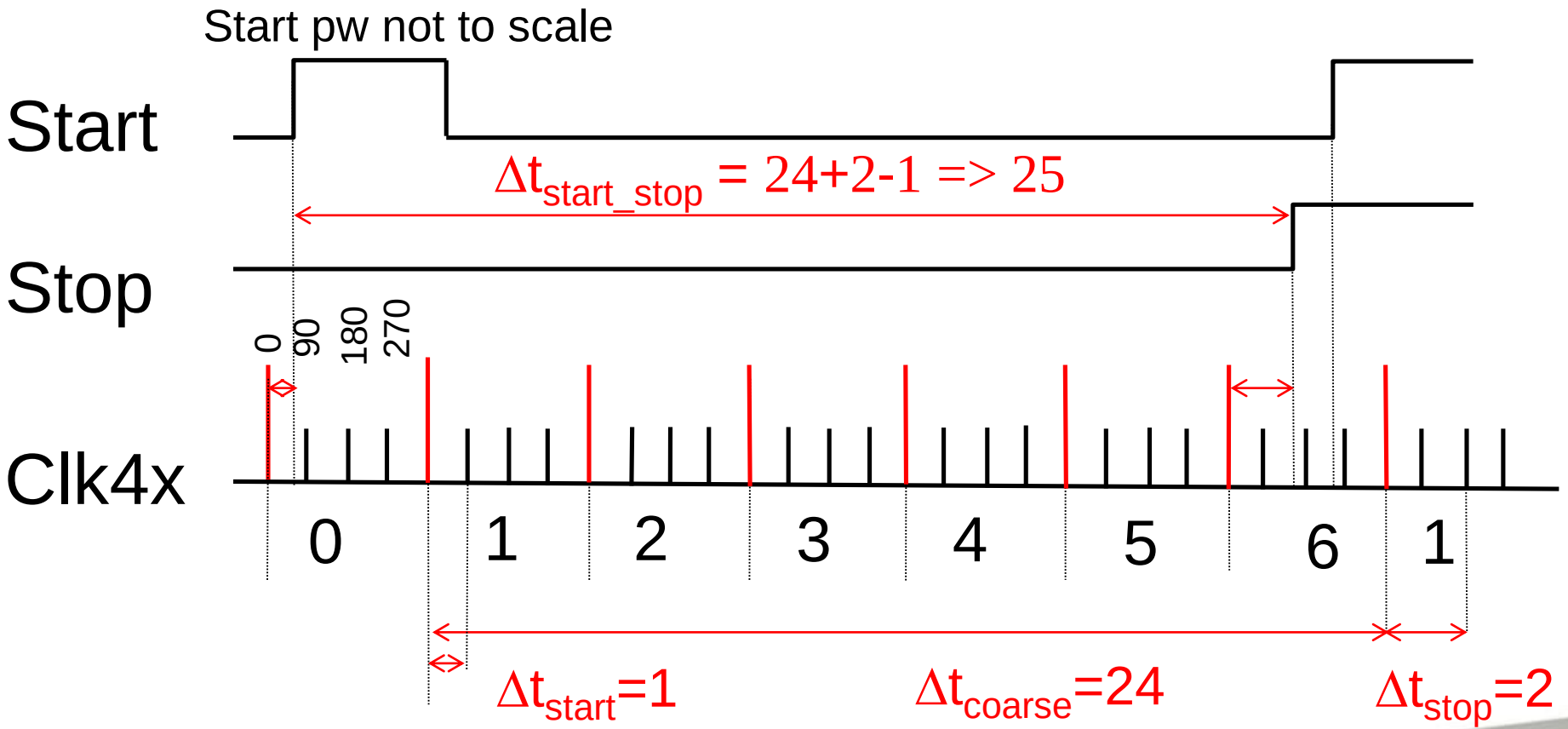
Multi-Phase_4x 1



Multi-Phase_4x 2



Multi-Phase_4x 3



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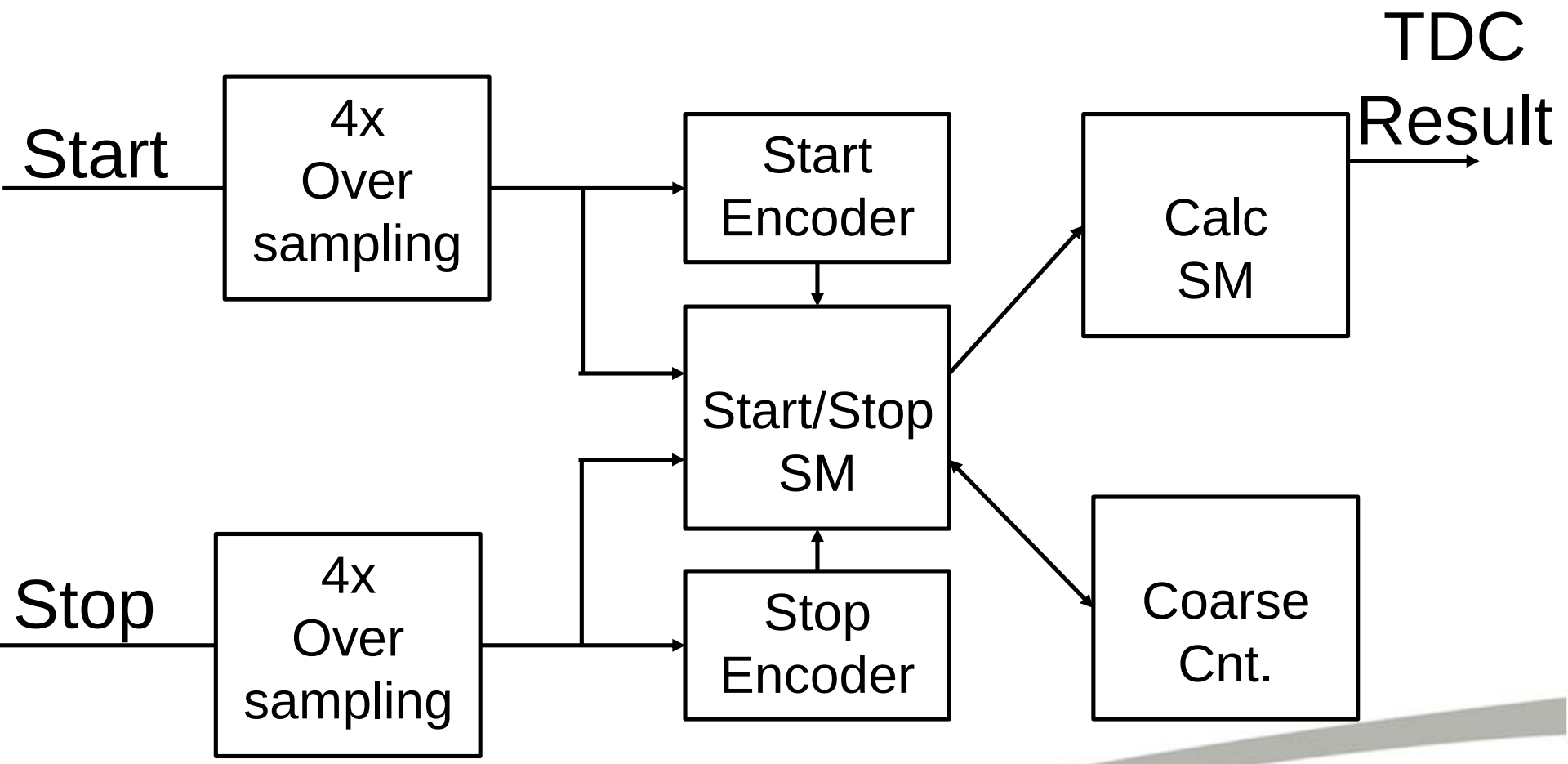
Neda TDC Block Diagram



Questions

- Clk that generates clk0 (300MHz), correlated to ADC clk.
- Start/Stop minimum repetition time.
- 5ns correction for odd samples.
- Samples before/after ZCO and TDC value association.
- Interface to Readout Blk.

Acknowledgements

- A.Balla et al., “Low resource FPGA-base Time to Digital Converter”.

- Tian Xiang et al., “A 56-ps multi-phase clock time-to-digital convertor based on Artix-7 FPGA”.

- Zhong Qi et al., “A high precision TDC based on a multi-phase clock”

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- Overall- Ian Lazarus
- Vhdl/Testing - Liam McNicholl
- Vhdl - Mos Kogimtzis