

# NUMEXO2 workshop

V6 IPs for NEDA processing

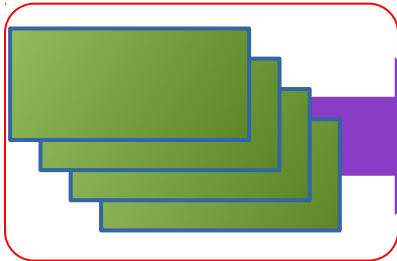
Debrecen, Hungary, 29th November, 2016

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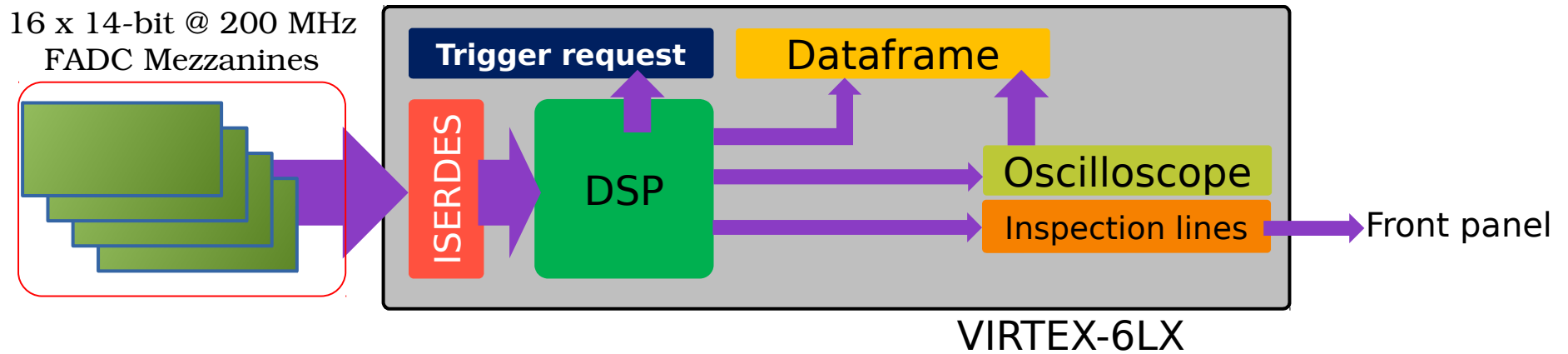
# NUMEXO-2 general block diagram

16 x 14-bit @ 200 MHz  
FADC Mezzanines

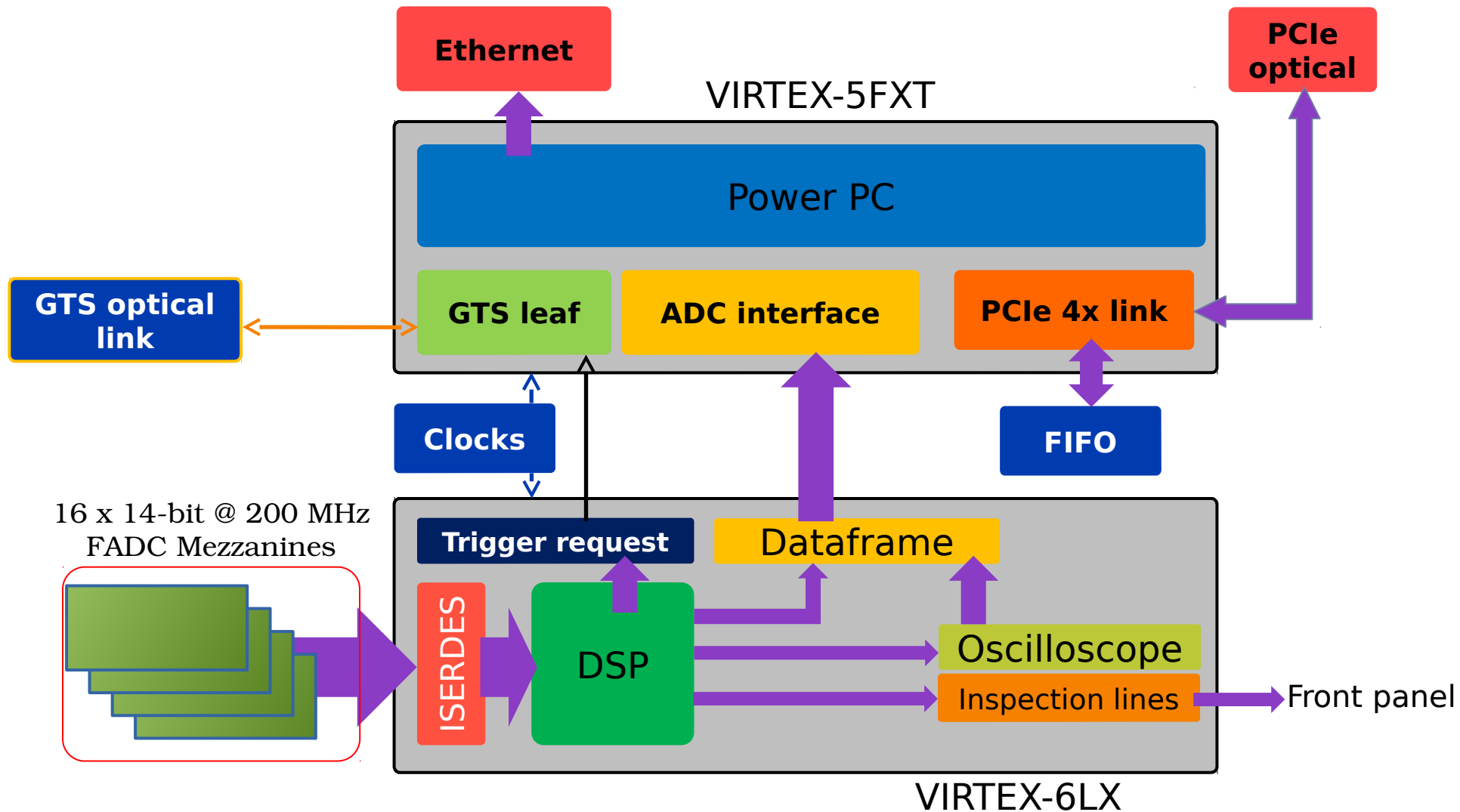


VIRTEX-6LX

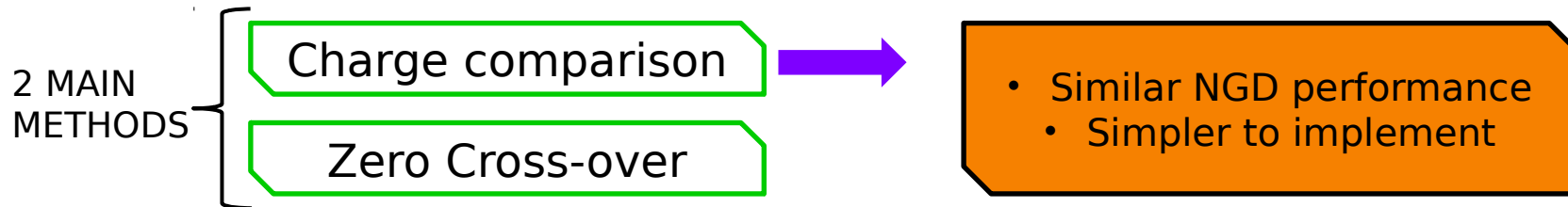
# NUMEXO-2 general block diagram



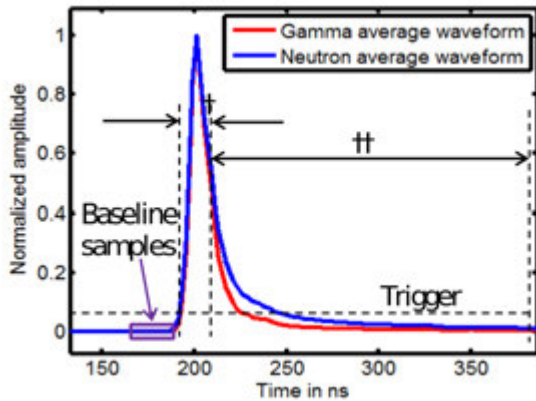
# NUMEXO-2 general block diagram



# PSA



## Algorithm

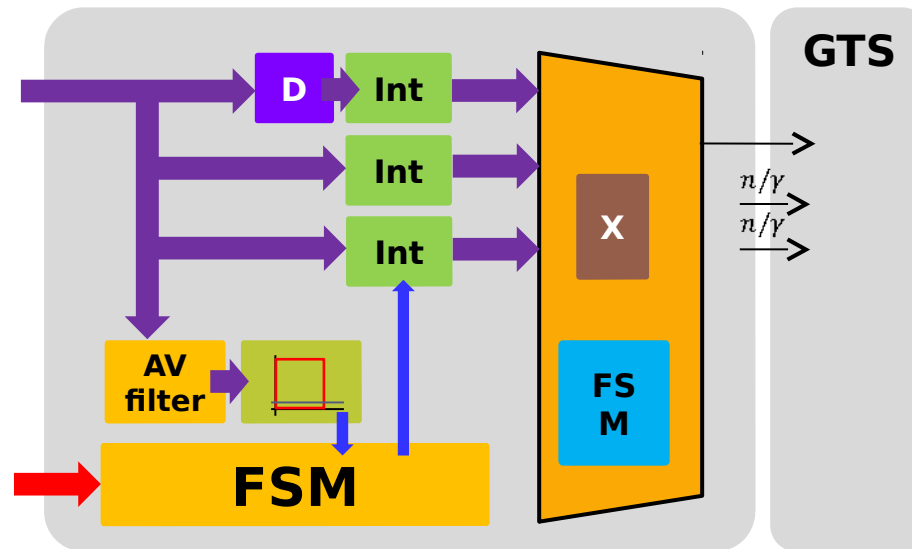


$$\hat{\delta} = \frac{\hat{I}_s}{\hat{I}_f} = \frac{\sum_{n=\alpha+1}^{\beta+\alpha} v(n) - \bar{I}_b}{\sum_{n=1}^{\alpha} v(n) - \bar{I}_b}$$

$$T_{req} = 1 \text{ if } \hat{I}_s \geq \delta_t \hat{I}_f \text{ (neutron)}$$

$$T_{req} = 0 \text{ if } \hat{I}_s < \delta_t \hat{I}_f \text{ (gamma)}$$

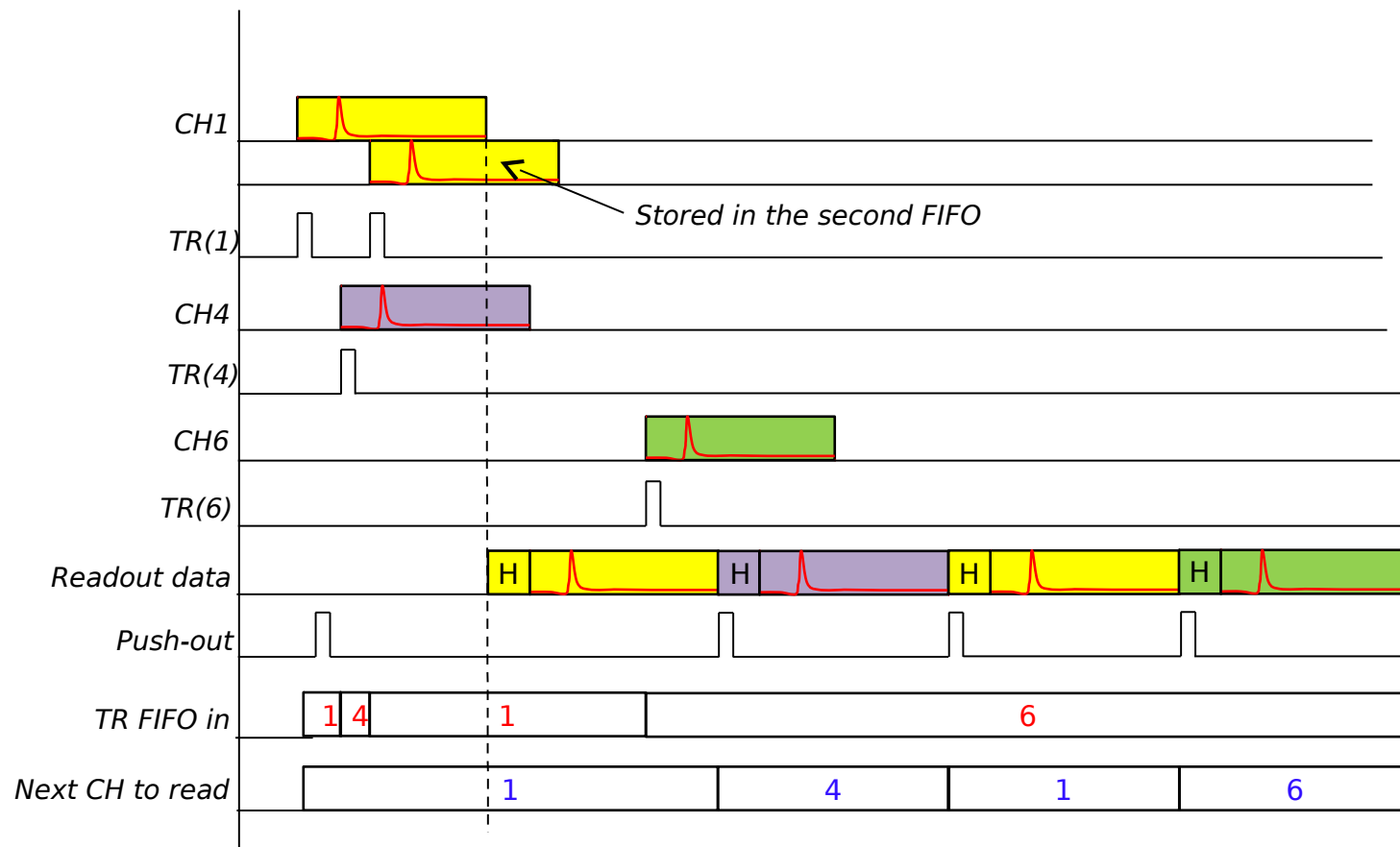
## Implementation



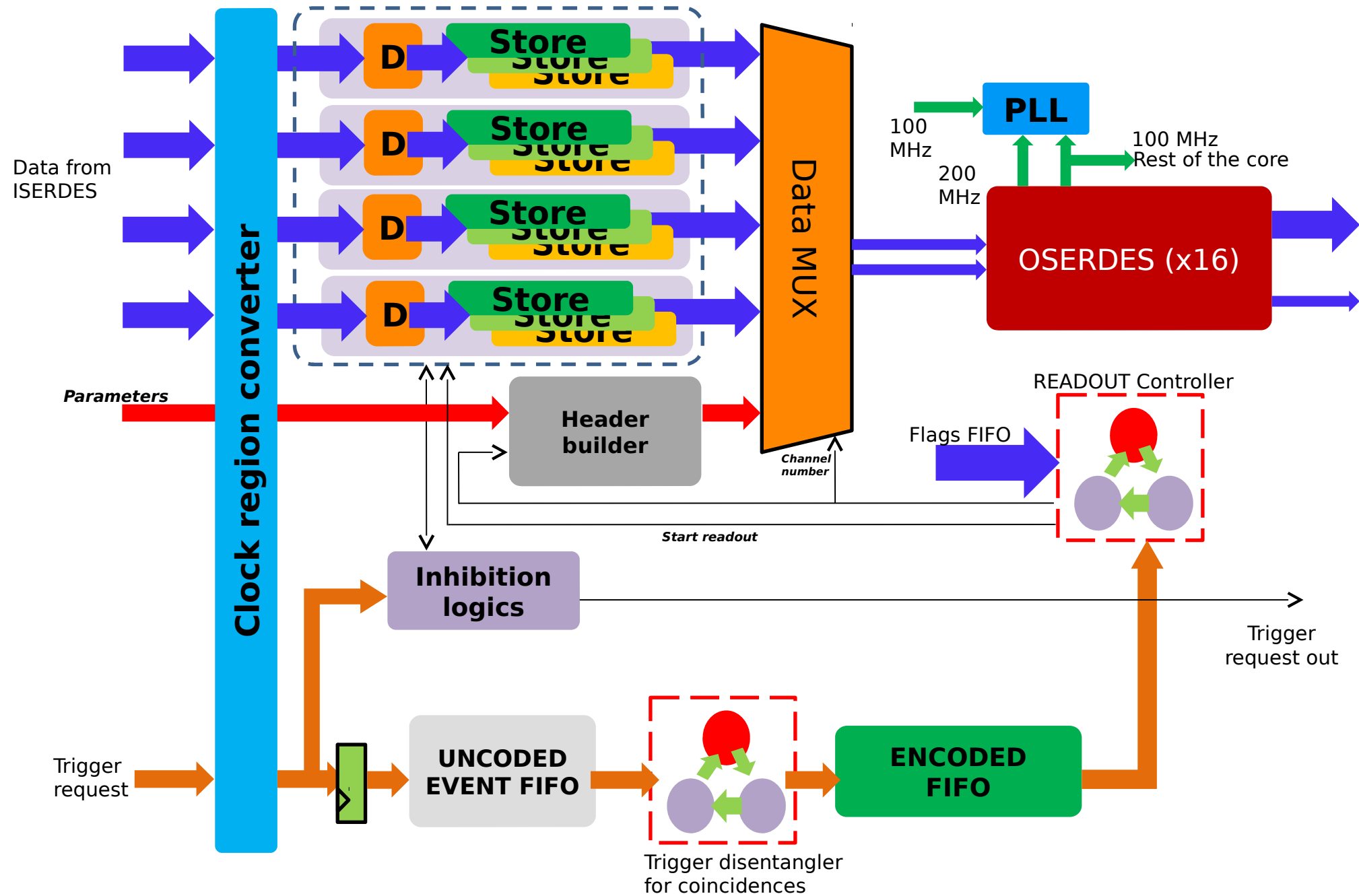
# Data readout example (so that you don't get lost in the mess...)

Example of readout in case of simultaneous events

- The readout order is preserved according to the arrival order
- Each channel contains three independent FIFOs to lower the probability that an event will not be read out
- In case of memory saturation, the inhibition logics doesn't send the TR and the correlation between TR and events is preserved



# Data readout V6-V5

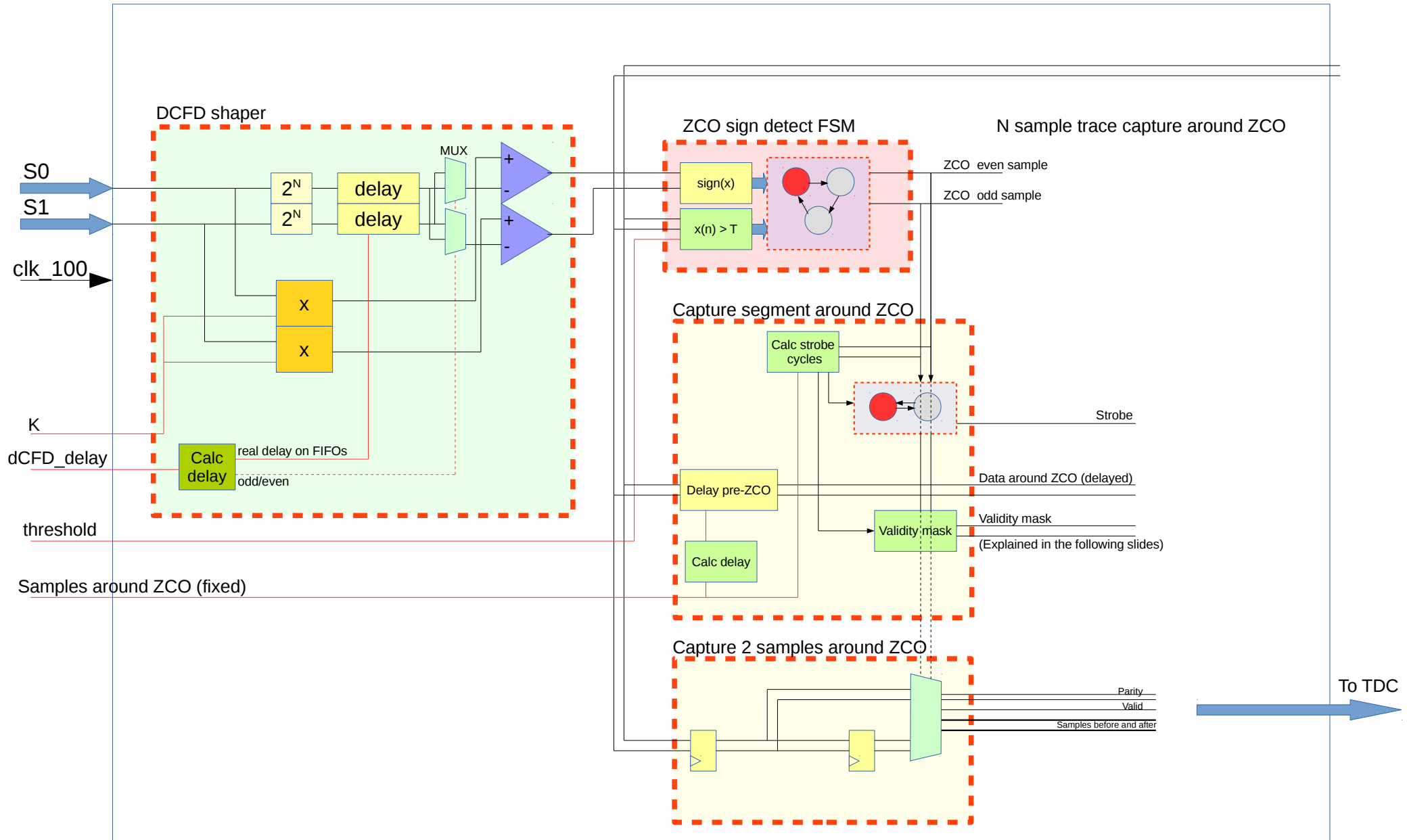




# Data readout frame format

Filed name	Bytes	Desription
metaType	1	Set to 0x02 (binary 00000002) big endian, basic frame, unit block size of $2^2=32$ bits
frameSize	3	Total size of the Frame (including Header) expressed in block units of 32 bits
subsystemNumber	1	Number of the detector subsystem in the system
frameType	2	The NR-Frame frameType code is set to 0x12 The NC-Frame frameType code is set to 0x13
revision	1	Set to 0, because it corresponds to revision 0 of the NR-Frame data format
headerSize	2	Must be expressed as an integer number of units blocks defined in the metaType field which is 32 bits. So the value of the headerSize is set to 7 (0x7)
itemSize	2	Size of a data item in bytes. It is set to 2
nItems	4	Total number of items in the frame. Because of the 32bits data readout FIFO of NUMEXO2, the number of samples has to be even
channelId	2	The channel Id is composed of a Board index in the system from which the frame originates (bits 15:5) and of the channel number in the board (bits 4:0)
eventNumber	4	Attached by the GTS in the Virtex-5
timeStamp	6	Attached by the GTS in the Virex-5
rawData	N	Waveform data

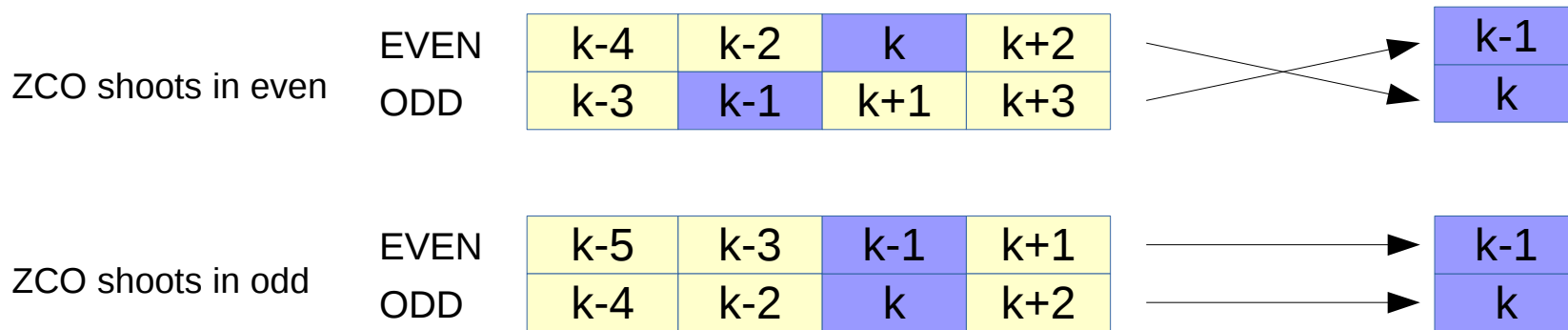
# CFD



# CFD interlacing cases and interface to the TDC

Example for 2 samples around the ZCO point

K-th sample is the first inverted sign, (k-1)th, instead is its precedent sample

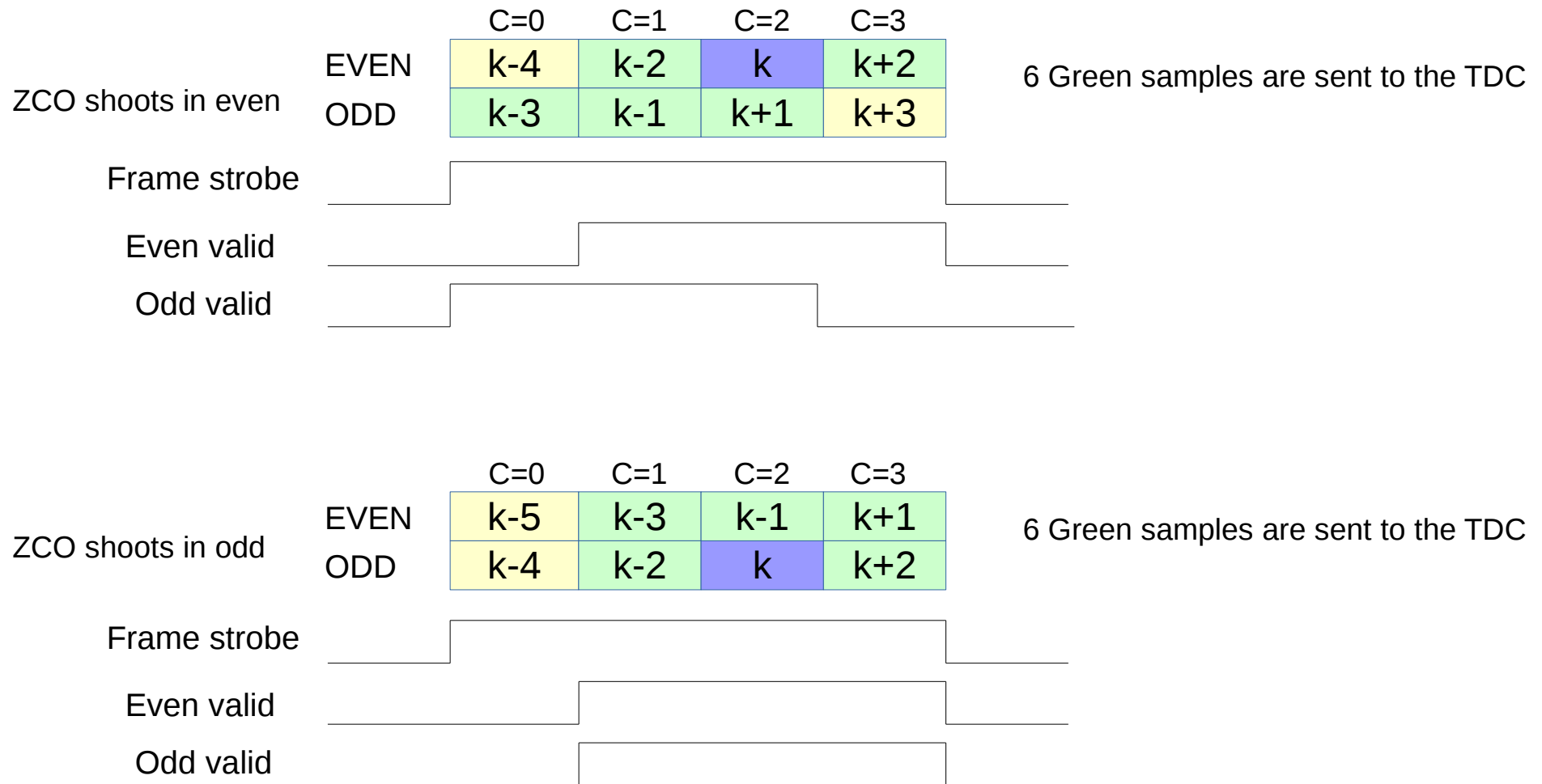


## Considerations

- A 'valid signal' is enabled at the same time whenever the ZCO should be dispensed
- Two extra signals are used to provide a clue about the polarity (either if the shot occurred in even or odd sample)

# CFD interlacing cases and interface to the TDC

Example for more than 2 samples around the ZCO point (higher order interpolation)



The frame strobe pulse width signal doesn't depend on the parity of the ZCO shot, it only depends on the number of samples around the ZCO sample.

# Registers

- **PSA** registers to be commanded independently (16 x each):
  - Alpha (fast component of the CC)
  - Beta (slow component of the CC)
  - Delta (discrimination parameter)
  - Use/bypass PSA mode
  - Threshold for the threshold detector
- **CFD** registers (16 x each):
  - Parameter K (fraction)
  - Delay CFD
  - Threshold
- **TDC** registers
- Spare registers

# Experimental setup



# Experimental setup

Single-ended to differential module

- Using a prototype with 3/4 channels working (a potentiometer is missing)
- The current production needs a greenlight from the swedish administration to proceed

V6 firmware

- ISERDES → OK
- PSA → Seems that it is working but we must verify its performance with data
- CFD → Ongoing test
- Readout unit V6-V5 → OK

Still...

- PCIe bridge LINCO2 shows problems to detect the link.